EAST - [10747680.wsp:1]

File View Edit Tools Window Help

- Drafts
  - BRS:
- Pending
- Active
  - L1: (3085) semiconductor and spacer$1 and protective near layer
  - L2: (6741) spacer$1 and protective near layer
  - L4: (58) 2 and ((spacer$1 with (vertical near sidewall)) or (vertical near spacer$1) or (rectangu...
  - L6: (77) 2 and ((spacer$1 with (vertical near sidewall)) or (vertical near spacer$1) or (rectangu...
  - L7: (49518) semiconductor and spacer$1
  - L8: (450) 7 and (vertical near spacer$1 rectangular near spacer$1 I-shape near spacer$1 I near sh...
  - L9: (1) ("6440875").PN.
  - L10: (2) ("0625764").PN.
  - L11: (1) ("6625764").PN.
  - L12: (1) ("6323519").PN.
  - L3: (12) 2 and (spacer$1 with (vertical near sidewall))
  - L5: (58) 2 and ((spacer$1 with (vertical near sidewall)) or (vertical near spacer$1) or (rectangu...
  - L13: (1) "20050146059"
- Failed
  - 2 and ((spacer$1 with (vertical near sidewall)) or (vertical near spacer$1 (rectangular near shap...
  - 2 and ((spacer$1 with (vertical near sidewall) or (vertical near spacer$1) or (rectangular near s...
- Saved
- Favorites
- Tagged (0)
- UDC
- Queue
- Trash

Search | List | Browse | Queue | Clear

DBs | US-PGPUB; USPAT; USOCR | Plurals

Default operator: OR | Highlight all hit terms initially

7 and (vertical near spacer$1 rectangular near spacer$1 I-shape near spacer$1 I near shape near spacer$1 rectangular near shape near spacer$1)

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20050146059 A1	20050707	7	Method for forming rectangular-shaped spacers for semiconductor devices		257/900
2	☐	☐	US 20050139933 A1	20050630	10	Semiconductor devices and methods for fabricating the same	257/370	438/234
3	☐	☐	US 20050136676 A1	20050623	13	Method of forming a floating gate for a split-gate flash memory device	438/703	
4	☐	☐	US 20050124104 A1	20050609	25	Methods of fabricating semiconductor device having T-shaped gate and L-shaped spacer	438/197	
5	☐	☐	US 20050122464 A1	20050609	6	One-drop fill spacerless process for liquid crystal cell on a silicon backplane or microdisplays	349/190	349/156
6	☐	☐	US 20050116293 A1	20050602	34	Transistor structure, memory cell, DRAM, and method for fabricating a transistor structure in a semiconductor substrate	257/349	
7	☐	☐	US 20050098820 A1	20050512	13	Method to remove an oxide seam along gate stack edge, when nitride space formation begins with an oxide liner surrounding gate stack	257/314	257/316; 257/E21.682; 257/E27.103;
8	☐	☐	US 20050085064 A1	20050421	30	Sacrificial metal spacer damascene process	438/622	257/E21.579
9	☐	☐	US 20050082963 A1	20050421	268	Image formation apparatus	313/493	313/310
10	☐	☐	US 20050067620 A1	20050331	8	Three dimensional CMOS integrated circuits having device layers built on different crystal oriented wafers	257/67	257/74; 257/E27.026; 257/E27.112;
11	☐	☐	US 20050064635 A1	20050324	11	METHOD FOR AVOIDING OXIDE UNDERCUT DURING PRE-SILICIDE CLEAN FOR THIN SPACER FETs	438/184	

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